

# SNAP

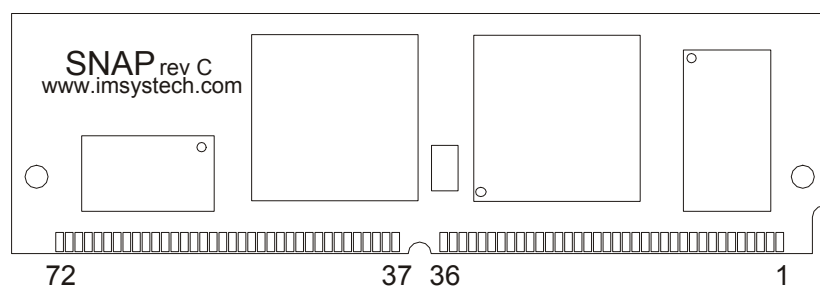
## Simple Network Application Platform

SNAP is an Internet-ready, Java powered plug & play reference platform. It is ideal for remote control, data processing and managing of everything from small sensors to advanced surveillance factory equipment. The Java 2 Micro Edition-CLDC runtime environment speeds up and simplifies your software development.

### FEATURES

- Standard 72-pin SIMM form factor
- Plugs into TINI compatible socket boards
- SUN certified J2ME-CLDC
- SNAP runtime environment
- High performance
  - Native Java execution
  - IEEE 754 floating point acceleration
- Extensive I/O capabilities through Java APIs
  - Three serial ports
  - Dual 1-Wire<sup>®</sup> net interfaces
  - CAN (Controller Area Network)
  - High-speed I<sup>2</sup>C bus and SPI
  - General-purpose digital I/O
- 10/100Base-T Ethernet
- TCP/IP stack
- Real time clock and calendar
- 2 Mbytes flash memory
- 8 Mbytes DRAM
- Single +5V power supply
- Connector for optional C/Java/assembler debug SW
- Wide operating temperature range, -20° to +70° C

### PIN ASSIGNMENT

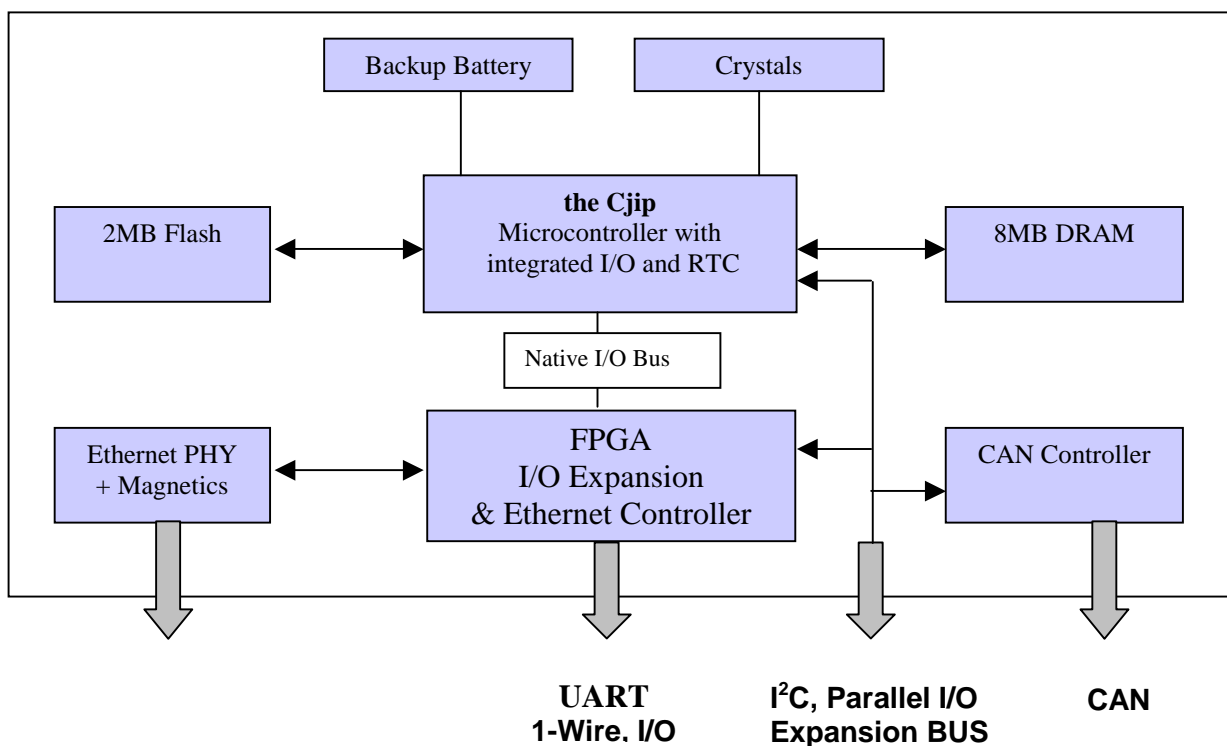


## PIN DESCRIPTION

PIN	SIGNAL NAME	TYPE	DESCRIPTION
67, 68, 69, 70	VCC	-	+5V supply $\pm$ 5%
3,6,7	GND	-	Ground.
9	VPP	-	+12V supply for EPROM programming via the OWIO pin. Must be connected to +5V if EPROM programming is not needed, or the on-board DS2480 device might break.
13, 62..60, 44..37, 33..36, 57..54	A19..A0	O	Address lines.
46..53	D7..D0	I/O	Data lines.
12	CE0	O	Chip enable 0. Address range: 0x00000-0xFFFFF
45	RCE0	I	General purpose input pin.
31	CE3	O	Chip enable 3. Address range: 0x300000-0x3FFFFFF
27	PCE3	O	Peripheral chip enable 3. Address range: 0xB00000-0xBFFFFFF
28	PCE2	O	Peripheral chip enable 2. Address range: 0xA00000-0xAFFFFFF
29	PCE1	O	Peripheral chip enable 1. Address range: 0x900000-0x9FFFFFF
30	PCE0	O	Peripheral chip enable 0. Address range: 0x800000-0x8FFFFFF
32	PSEN	O	Program store enable.
16	RD	O	Read strobe.
58	WR	O	Write strobe.
63, 64	ETH3, ETH6	I	10/100Base-T differential input pair.
65, 66	ETH2, ETH1	O	10/100Base-T differential output pair.
19	TX232	O	Serial 0 transmit line, RS-232 levels.
20	RX232	I	Serial 0 receive line, RS-232 levels.
25	DTR232	I	RS232 level reset input. Used by development system to take control over the module. Active "high" (positive voltage).
21	TX	O	Serial 0 transmit line, TTL levels.
22	XRX0	I	Serial 0 receive line, TTL levels.
14	TX1	O	Serial 1 transmit line, TTL levels, or alternate I2C SCL line.
15	XRX1	I	Serial 1 receive line, TTL levels, or alternate I2C SDA line.
4	TX4	O	Serial 4 transmit line, TTL levels. Available if the primary 1-Wire bus is not used (EN2480 low).
5	RX4	I	Serial 4 receive line, TTL levels. Available if the primary 1-Wire bus is not used (EN2480 low).
10	CTX	I/O	CAN bus TX line, standard I2C SCL line, or general-purpose input/output.
11	CRX	I/O	CAN bus RX line, standard I2C SDA line, or general purpose input/output.

8	OWIO	I/O	Primary (external) 1-Wire bus I/O pin with EEPROM programming capability, controlled by DS2480.
17	INTOW	I/O	Secondary (internal) 1-Wire bus I/O pin. Not tolerant to EEPROM programming voltage.
26	EN2480	I	Active high enable input for the on-board DS2480 controlling OWIO. When low, TX4 and RX4 are enabled instead, unless they are grounded in the motherboard socket.
24	CPURST	I/O	Active high CPU reset input, pulled low through 22 kΩ on-board. Also driven high when the CPU is reset by other means.
18	SMCRST	O	Active high peripheral reset.
23	EXTINT	I/O	Active low/falling edge triggered interrupt input, pulled high through 20-90 kΩ. Can also be used as general-purpose input/output pin.
71	OUT1	O	General-purpose output pin. Can also be used as RTS for hardware flow control on serial 0, 1 or 4.
72	OUT2	I/O	General-purpose input/output pin. Can also be used as DTR for hardware flow control on serial 0, 1 or 4.
2	IN1	I	General-purpose input pin. Can also be used as CTS for hardware flow control on serial 0, 1 or 4.
59	IN2	I	General-purpose input pin.
1	IN3	I/O	General-purpose input/output pin. Can also be used as DCD for hardware flow control on serial 0, 1 or 4.

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
Voltage on any pin Except for the following pins: RX232, TX232, DTR232	-0.3	$V_{CC}+0.3$	V
ETH1 ETH2	-30	+ 30	V
ETH3 ETH6		+125	V
$V_{pp}$	$V_{CC}$	+12.25	V
OWIO	-0.3	$V_{pp}$	V
Operating Temperature	-40	+70	°C
Storage Temperature	-55	+85	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	$V_{CC}$	4.75	5.0	5.25	V
Ambient Temperature	$T_{AMB}$	-20	+20	+70	°C

## DC ELECTRICAL CHARACTERISTICS

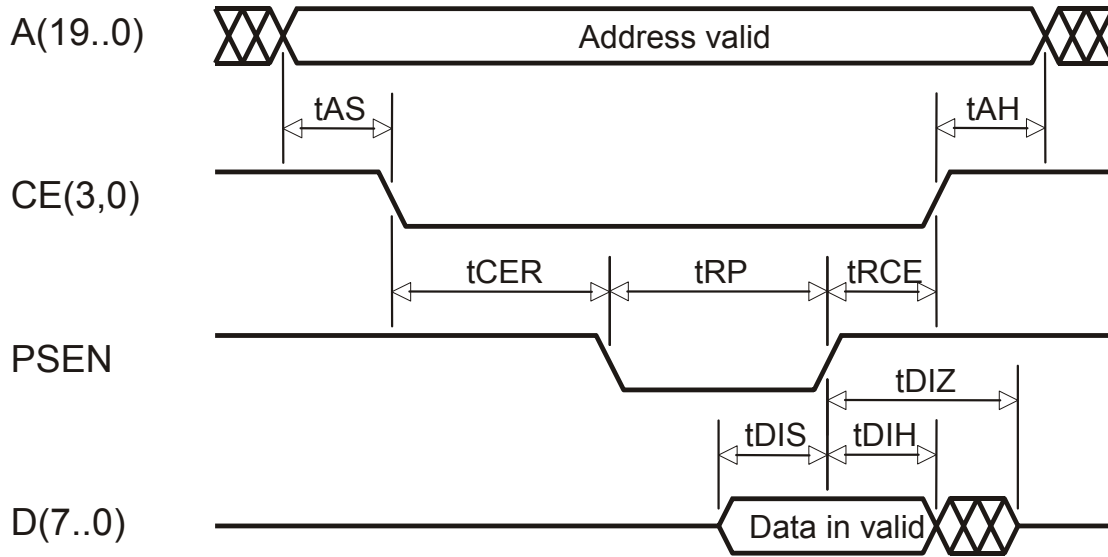
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Output Low Voltage @ $I_{OL} = 2\text{mA}$	$V_{OL}$			0.4	V
Output High Voltage @ $I_{OH} = -2\text{mA}$	$V_{OH}$	2.4			V
Input Leakage Current $0 < V_{IN} < V_{CC}$	$I_{IL}$			75	$\mu\text{A}$
Reset Trip Point	$V_{RST}$	4.5			V
Supply Current Active Mode	$I_{CC}$			340 <sup>1)</sup>	mA
Output Leakage Current $0 < V_{IN} < V_{CC}$	$I_{OL}$			140	$\mu\text{A}$

<sup>1)</sup> 100 Mbps Ethernet active.

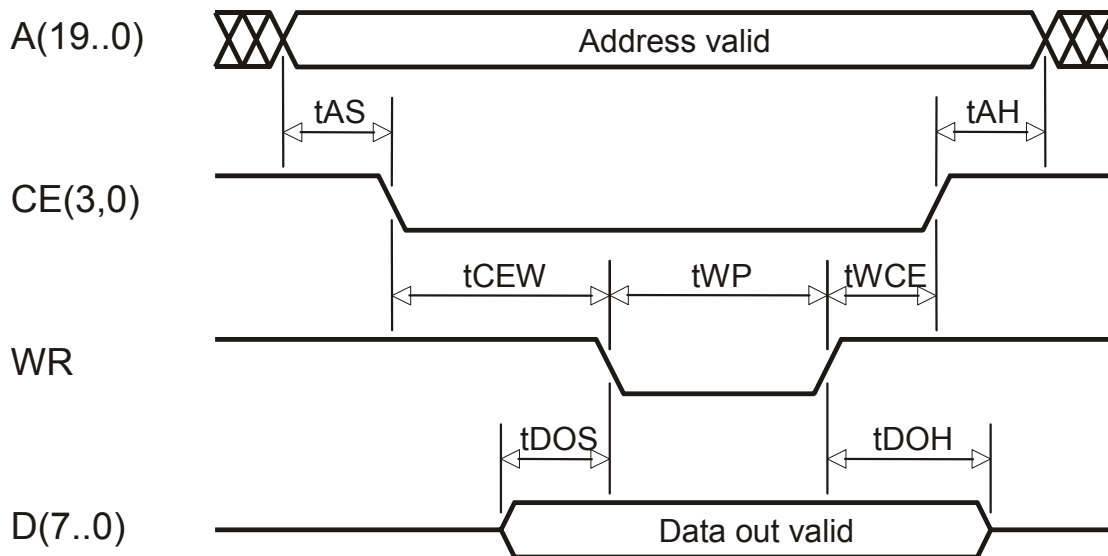
## AC ELECTRICAL CHARACTERISTICS

PARAMETER	NAME	MIN	MAX	UNIT	STRETCH VALUE
Internal oscillator cycle time	tC	12.5 ± 130 ppm		ns	
Address setup time before CE(3,0) or PCE(3..0) low	tAS	2		tC	
Address hold time after CE(3,0) or PCE(3..0) high	tAH	6		tC	
CE(3,0) or PCE(3..0) low to PSEN or RD low	tCER	4 21		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
CE(3,0) or PCE(3..0) low to WR low	tCEW	6 23		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
PSEN or RD low pulse width	tRP	4 C <sub>ST</sub> *9 + 1		tC	C <sub>ST</sub> = 0 1 ≤ C <sub>ST</sub> ≤ 7
WR low pulse width	tWP	4 C <sub>ST</sub> *9 + 1		tC	C <sub>ST</sub> = 0 1 ≤ C <sub>ST</sub> ≤ 7
PSEN high to CE(3,0) high or RD high to PCE(3..0) high	tRCE	4 13		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
WR high to CE(3,0) or PCE(3..0) high	tWCE	2 11		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
Data in setup time before PSEN or RD high	tDIS	10		ns	
Data in hold time after PSEN or RD high	tDIH	0		ns	
PSEN or RD high to data in floating	tDIZ		10 19	tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
Data out setup before WR low	tDOS	2 19		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7
Data out hold time after WR high	tDOH	4 13		tC	0 ≤ C <sub>ST</sub> ≤ 3 4 ≤ C <sub>ST</sub> ≤ 7

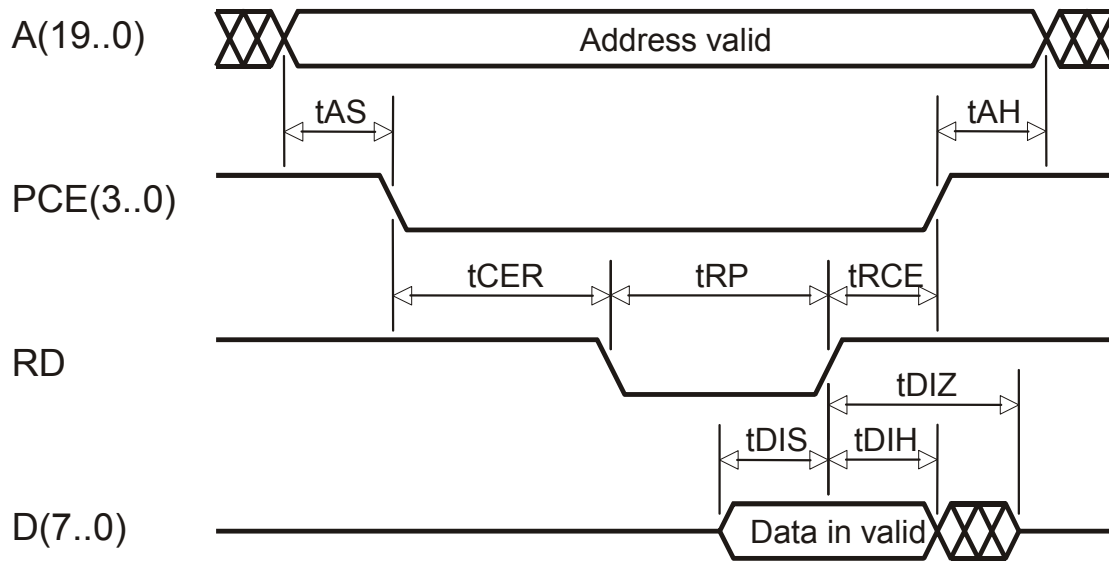
## CE READ CYCLE TIMING



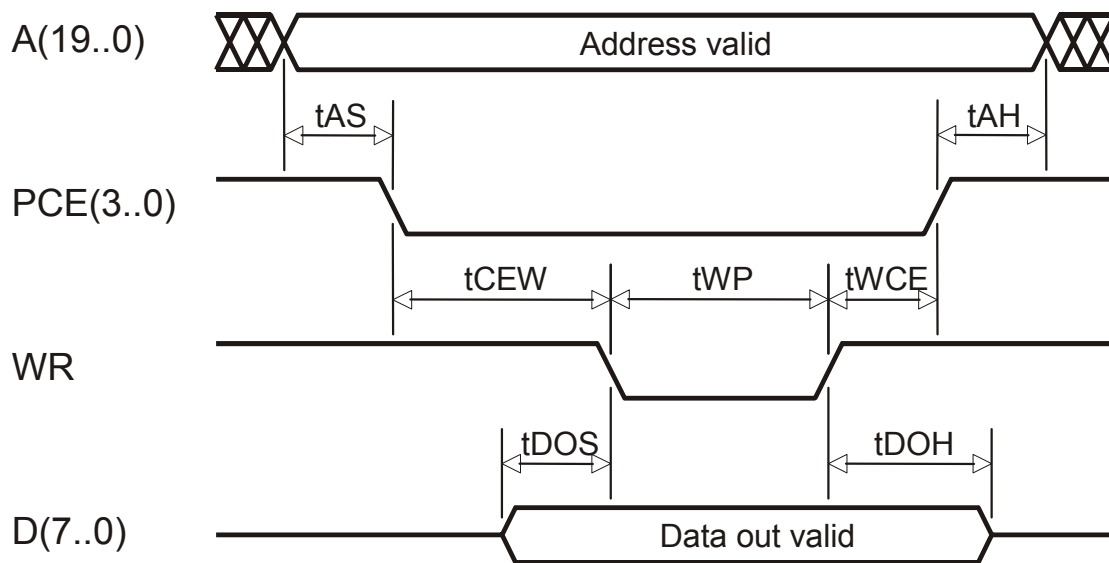
## CE WRITE CYCLE TIMING



## PCE READ CYCLE TIMING



## PCE WRITE CYCLE TIMING



## APPLICATION INFORMATION

### MEMORY ARCHITECTURE

The memory on the SNAP is divided into two parts, two megabytes of serial flash memory and eight megabytes of EDO DRAM.

The flash serves as secondary memory (like a hard disc drive) and contains firmware and file storage. All program and data files are stored here, but the processor never executes directly from the flash. Part of the flash is write-protected to ensure that boot loaders and basic firmware is never overwritten by mistake. More space for file storage can be provided by connecting memory to the parallel expansion bus.

The DRAM is used as primary memory, and is connected directly to the processor using a dedicated high-speed bus. All code is executed from this memory, after being loaded from flash. The garbage-collected heap as well as all other dynamic data is located here. File system data is also cached in DRAM to avoid unnecessary writes to the flash. The primary memory cannot be expanded on the socket board.

Since neither on-board flash nor DRAM is connected to the processor via the parallel expansion bus, the entire address range provided by the edge connector is available for interfacing additional peripheral devices and memory on the socket board. This applies to the CE address space (addresses 0x000000-0x0FFFFFF and 0x300000-0x3FFFFFF) and the PCE address space (addresses 0x800000-0xBFFFFFF), totaling six megabytes of I/O address space. Devices connected to the parallel expansion bus are accessed through the DataPort class, or – in the case of memory devices – through standard file I/O operations.

Additional memory devices on the socket board should preferably be connected to CE0, mapping into the first megabyte of I/O address space. There is a small performance penalty in using PCE space compared to CE space. If no devices are mapped into PCE space, the four peripheral chip select signals PCE(3..0) are available as general-purpose I/O pins.

### STRETCHED BUS CYCLES

The bus cycles on the parallel expansion bus can be stretched to allow interfacing of slow memory or peripherals. There are eight stretch settings ( $C_{ST}$ ) numbered from 0 to 7, with 0 being the fastest.

The effect of the stretch setting on the bus timing can be seen in the AC characteristics section earlier in this document. The timing in each stretch setting is tailored to match the corresponding timing on the TINI<sup>®</sup> module as closely as possible, without ever being tighter. It should therefore always be possible to communicate with a device on a socket board using the same stretch setting as is used for that device on the TINI.

The stretch setting for a certain address or address range is set by the user program using the DataPort class

## FIRMWARE LOAD

### SERIAL BOOTSTRAP LOADER

To set up the flash and download the SNAP firmware, a bootstrap loader exists. The bootstrap loader defaults to 115200 baud (which can be set to other values after boot). The bootstrap loader is downloaded into flash when the module is manufactured. The area of the flash where the loader is stored is write-protected.

The bootstrap loader will boot the FPGA, and detect if the snapdev.exe program is active on the serial port. The snapdev.exe is PC software used for SNAP firmware download. This program is available for download at <http://www.imsystech.com/snap/download>. If the bootstrap loader doesn't detect the snapdev.exe program, the default application will be loaded.

If the loading of the program fails, the yellow status LED (located close to the battery) will flash with a status code.

If the snapdev.exe program is detected, an application will be downloaded from the snapdev.exe program, which enables access to the flash through the serial port. The application provides a simple interface to setup the flash and download firmware.

### COMMAND SET

COMMAND	FUNCTION
B XXXX	Set baud rate
E, Q, R	Exit loader and reboot
F	Format flash (all data will be lost)
I	Print information about hardware
H, ?	Print help
L	Go into load mode
V	Print version information

### HANDLING INSTRUCTIONS

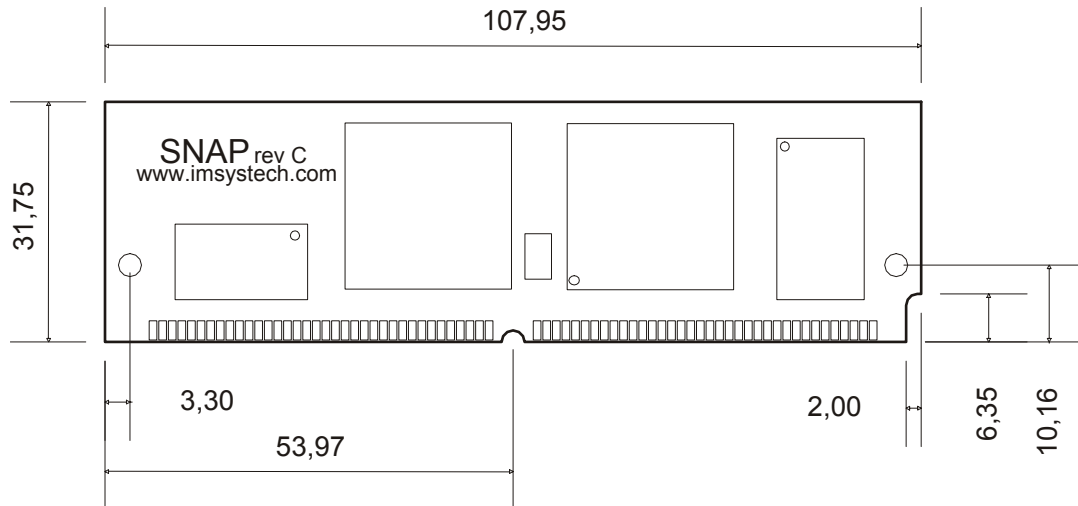
The SNAP module has been designed for ease of use and robustness, however Electrostatic Discharge, ESD, precautions should be observed when handling the module. The module should be stored in an anti-static bag or box when not mounted. When inserting the SNAP module into a socket, verify that power is not present.

VCC and GND connections should be checked before applying power. The input voltage shall be between 4.75 and 5.25 volts.

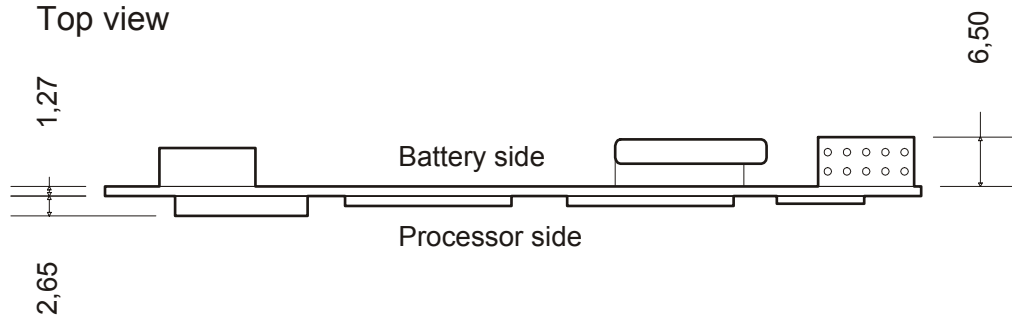
## PHYSICAL DIMENSIONS

Drawing unit: mm  
Drawing scale: 1:1

Processor side view



Top view



## Reference Design

SNAP can be used as a reference design in designing your own optimised OEM product. Design information, like schematics, is open and available at <http://www.imsystech.com/snap>.

## Development tools

Standard Java development tools can be used for building applications on SNAP. The advanced user, in need of writing native functions, can connect SNAP via a trace adapter to a PC based Integrated Development Environment, IDE. Through Imsys SNAP IDE, the developer can handle a mix of Java, C and assembler code.

# ORDERING INFORMATION

PRODUCT	PRODUCT NUMBER
SNAP Module	IM-SNAP-01
SNAP Development Environment	IM-SNAP-IDE-01